18-Channel, 16bits SPI-Bus to PWM Converter

General Description

The VAS6685 is a 18-channel SPI-bus to PWM converter optimized for RGB color LED lighting applications.

Each channel is independently programmable for a PWM duty cycle in programable steps(4096 to 65536 steps), synchronizing with the SYNCB signal by setting a group of registers.

Each output has 10mA sink/source capability and has the same PWM frequency.

The VAS6685 operates with a supply voltage range of 2.7V to 5.5V.

VAS6685 is available in a QFN4*4-28 package.

Features

- 18 channels
- Independent 16-bit PWM resolution for each channel
- 25MHz SCK input
- 25MHz PWM counter clock input
- SPI interface with SYNC
- Programmable PWM resolution
- Operating power supply voltage range of 2.7V to 5.5 V
- QFN4*4-28 package

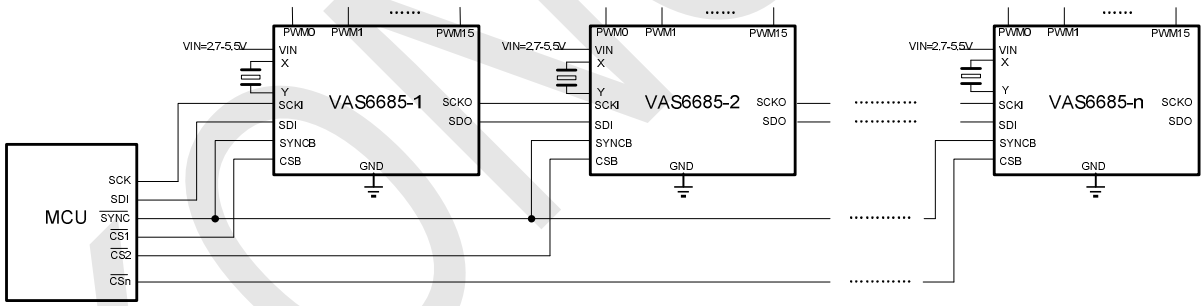
Ordering Information

Order Number	Package Type	Temp. Range
VAS6685IJ28E	QFN4*4	-40 °C to 85°C

Application

- RGB LED Lighting

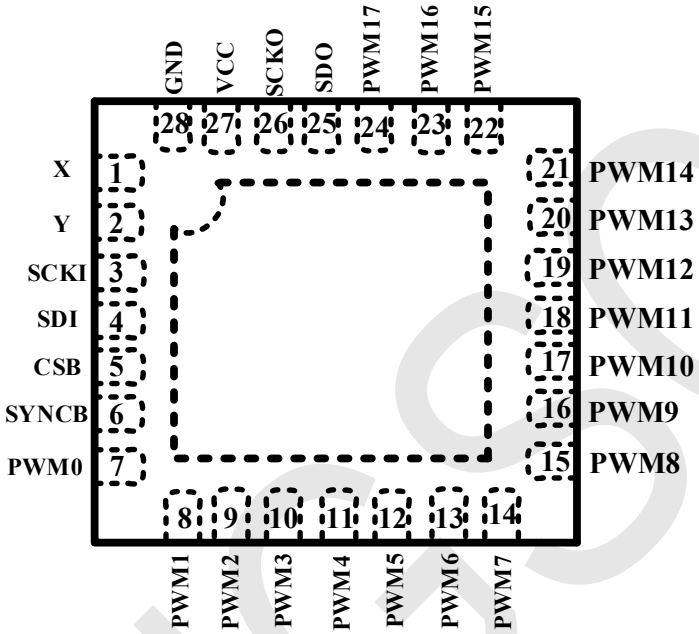
Typical Application Circuit



Block Diagram

Pin Configuration

QFN4*4-28



QFN4X4

PIN Description

PIN No.	PIN Name	DESCRIPTION
1	X	Connect to the crystal
4	Y	
3	SCKI	Serial interface Clock Input
4	SDI	Serial interface Data Input
5	CSB	Active Low Chip Select input
6	SYNCB	Active Low to disable PWM output, and a rising edge will PWM output
7~24	PWM[17:0]	The 16bit PWM output, default=0
25	SDO	Serial interface Data Output
26	SCKO	Serial interface Clock Output
27	GND	Ground
28	VCC	Supply Voltage input, the range is 2.7V to 5.5V

Absolute Maximum Ratings (Note1)

Parameters	Maximum Ratings
All PINs to GND	-0.3 to 6.0V
Operating temperature range	-40°C to +85°C
Junction temperature	-40°C to +150°C
Storage temperature range	-65°C to +150°C
ESD human body model	2000V

Note1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics(Note2)

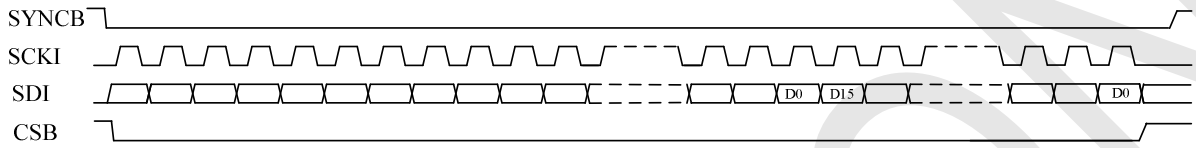
Symbol	Parameter	Conditions	SPEC			Unit
			Min	Typ.	Max.	
VIN	Power Supply Range		2.7		5.5	V
I_Q	Quiescent Supply Current	All outputs OFF		500		μA
Output Ports (PWM0 thru PWM17)						
I_{OUT}	Output current range	V_{CH}=1V			10	mA
PWM	PWM Resolution		12		16	bits
Y, SCKI, SDI, SCKO, SDO						
I_{LKG}	Input Leakage current	0V < V_{IN} < 5.5V		0.2	1	μA
V_{IH}	Input voltage logic high		1.4			V
V_{IL}	Input voltage logic low				0.8	V
SCKI, SDI, CSB, SYNC Timing						
f_{OSCI}	OSCI Input frequency		0		25	MHz
f_{SCKI}	Serial Data clock frequency		0		25	MHz
t_{PWCS}	Chip select pulse width			30		ns
t_{SUCS}	Setup time for signal			5		ns
t_{HDCS}	Hold time for signal			5		ns
t_{PWSCKI}	Serial Data clock pulse width			20		ns
t_{HDSCKI}	Serial Data clock hold time			5		ns
t_{SUSCKI}	Serial Data clock setup time			5		ns
t_{SUSYNC}	Setup time for signal			5		ns
t_{HDSYNC}	Hold time for signal			5		ns

Note 2: Production testing of the device is performed at 25°C. Functional operation of the device and parameters specified over other temperature range, are guaranteed by design, characterization and process control.

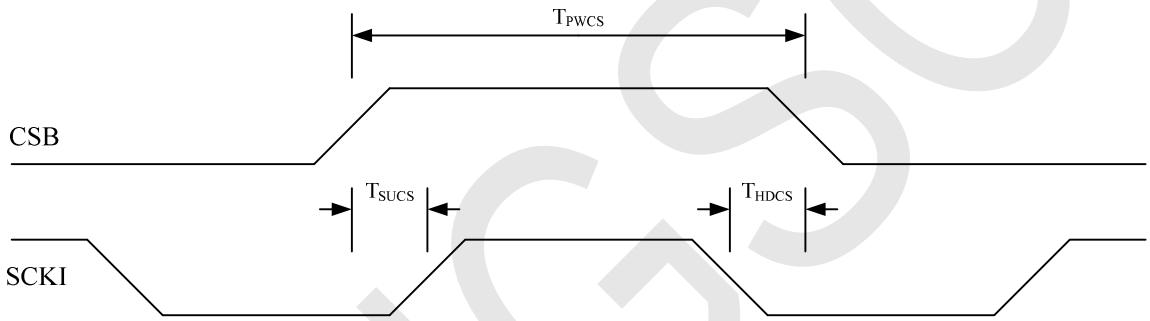
Typical Performance Characteristics

Application Information

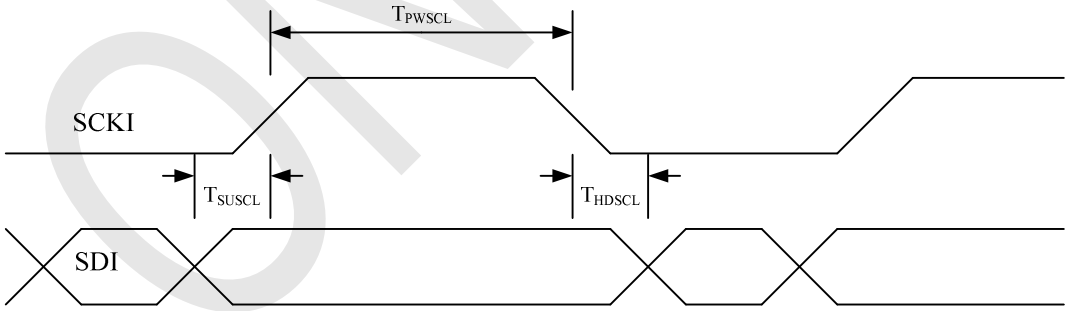
1. Timing Rules



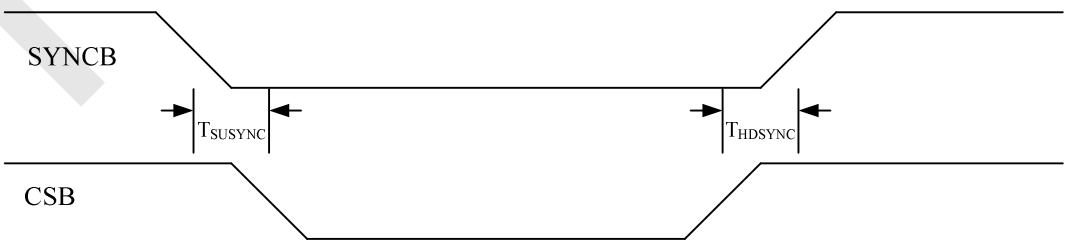
Data Input Timing Diagram



CSB and SCKI timing rule



SCKI and SDI timing rule



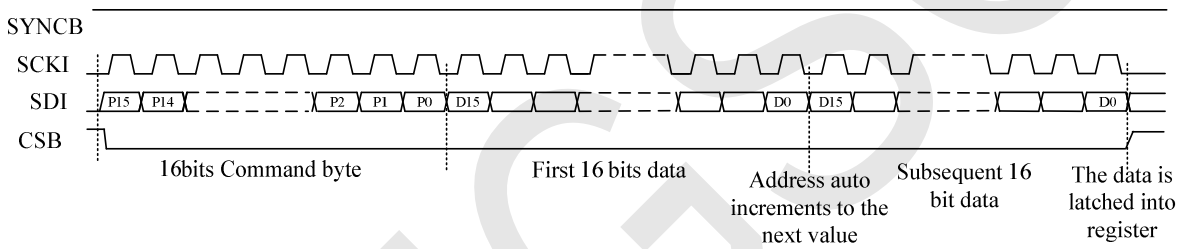
SYNCB and CSB timing rule

2. Writing to the VAS6685

To write data to any register of the VAS6685 use the following steps:

1） Take SCKI low, if it is not already low.
2） Take CSB low.
3） Set the SDI signal to the value of the bit to be clocked into the device.
4） Take SCKI high.
5） Take SCKI low.
6） Repeat steps 3 thru 5 until the last bit of data has been clocked into the device.
7） Take CSB high.

The VAS6685 interface can accept any starting address for the data. When writing to the PWM delay registers or the Configuration register the operation of the interface is independent of the SYNCB signal. However, when writing to the PWM registers, the data is not allowed to move to the outputs until both the CSB and the SYNCB signals have returned to a high state (see the Writing to the VAS6685 with SYNCB section). If the signal remains high during writes to the PWM setting registers, the data will transfer to the outputs at the rising edge of the signal and will take affect at the start of the next PWM sub-frame.

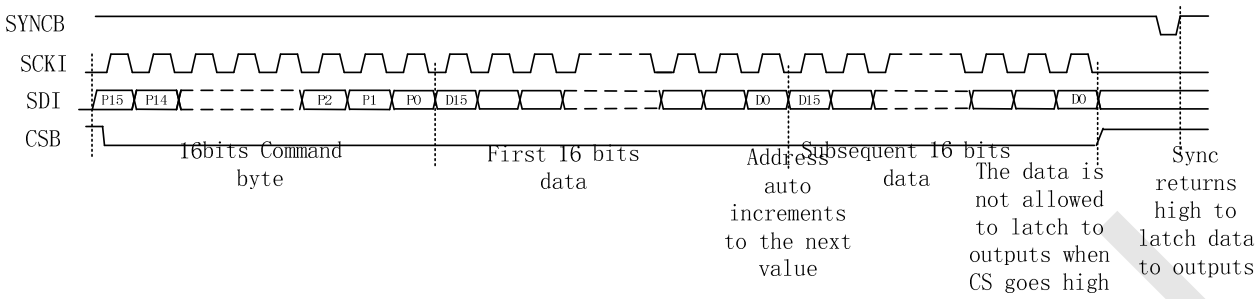


3. Writing to the VAS6685 with SYNCB

To write to the PWM registers of the VAS6685 using the SYNCB functions, use the following steps:

1) Take the SYNCB signal high. The output PWM is not affected by the SYNCB transitioning to high.
2) Take the SCKI low, if it is not already low.
3) Take the CSB low.
4) Set the SDI line to the correct state for the bit to be clocked into the device.
5) Take clock high. The data at SDI is shifted into the device on the rising edge of SCKI.
6) Return clock to low.
7) Repeat steps 4 thru 6 until the last bit of data has been shifted into the device.
8) Return CSB to high. The data is prevented from transferring to the PWM outputs because is still low.
9) Give SYNCB a nagtive pulse to latch the data to the outputs and restart the PWM counters at the beginning of the cycle.

The SYNCB signal will immediately restart the PWM counters on the rising edge regardless of where they are in the PWM cycle.



4. Register MAP

The VAS6685 receive integers frames from the hosts, there are 2 kinds of frame, 16bits command frame and 16bits PWM data frame.

The first 16bits must be command frame, the second 16bits are PWM data for a certain PWM output specified in command frame, the third 16bits are also PWM data, the corresponding PWM output address automatically plus one, and so as the fourth 16bits data and so on. The PWM registers:

Address	Description	Auto Increment Address
5‘b00000	Command	5‘b00001
5‘b00001	PWM0	5‘b00010
5‘b00010	PWM1	5‘b00011
5‘b00011	PWM2	5‘b00100
……	……	……
5‘b10000	PWM15	5‘b10001
5‘b10001	PWM16	5‘b10010
5‘b10010	PWM17	5‘b10011

PWM data format:

Bit	D[15:0]
Default	0000_0000_0000_0000
Note	16bit Data

The internal registers program the 16-bit register PWM setting for each output. With the 16-bit data, all output channels can be built with 65536 brightness scales. The duty cycle may be computed using the formula,

$$DutyCycle = \frac{1}{65536} * \left(\sum_{n=0}^{15} 2^n * D_n \right)$$

For example, if the data is 16’b0100_1000_0100_0000, the duty cycle will be:

$$DutyCycle = \frac{1}{65536} \times \left(2^{15} \times 0 + 2^{14} \times 1 + 2^{13} \times 1 + 2^{12} \times 0 + \cdots + 2^0 \times 0 \right)$$

$$= \frac{16384 + 2048 + 64}{65536} = \frac{18496}{65536}$$

5. Configration Register

The command registers format:

Bit	D[15:13]	D[12:0]
Name	PBS	Reserved
R/W	W	W
Default	3'b0	12'b0

PBS: PWM Bits Setting

100	12bits, 4096 steps
011	13bits, 8192 steps
010	14bits, 16384 steps
001	15bits, 32768 steps
000	16bits, 65536 steps

When the PBS is set, the input data LSBs(Least Significant Bit, depend on PBS value) are ignored automatically.

6. Choosing the PWM clock frequency

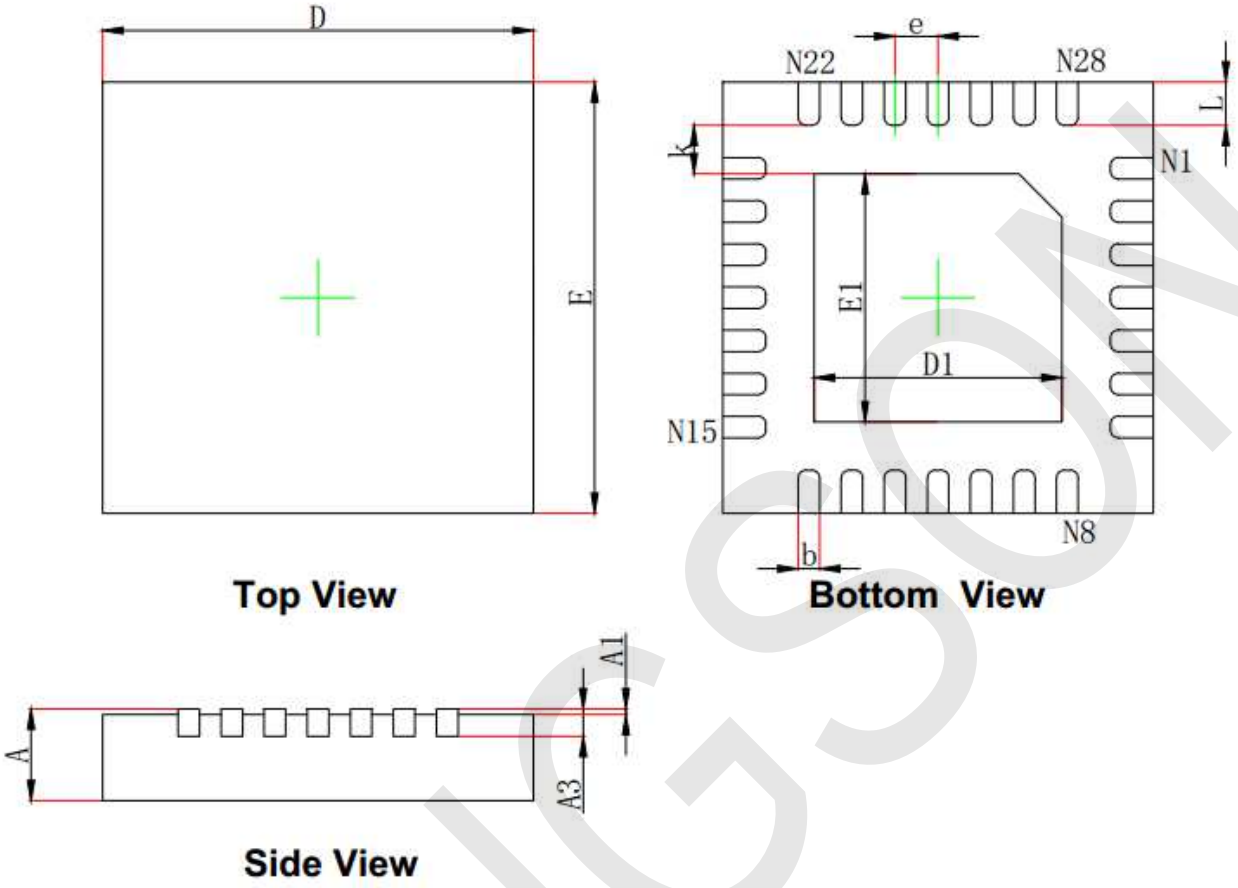
The period of the PWM waveform is determined by the externally generated PWM clock. The PWM clock frequency is computed starting with the desired refresh rate of the overall output waveforms. For a refresh rate of 600Hz, the required PWM clock frequency is computed as:

$$f_{PWMCLK} = 65536 \times 600Hz = 39{,}321{,}600Hz$$

If the register PBS are set, the f_{PWMCLK} need to change as well, for example, PBS=000

$$f_{PWMCLK} = 4096 \times 600Hz = 2{,}457{,}600Hz$$

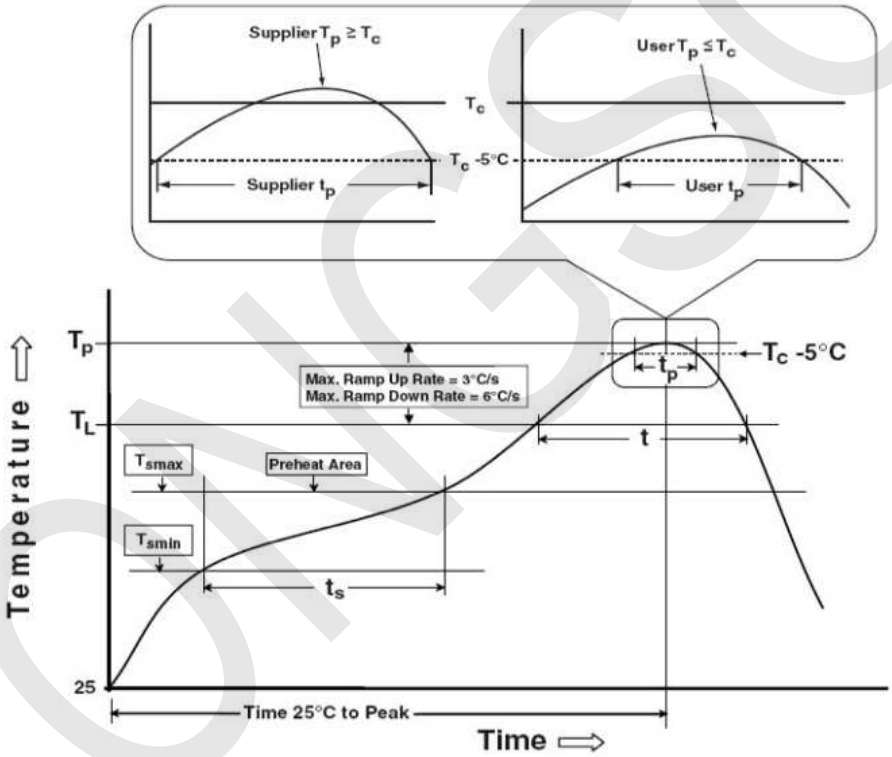
Package Information (QFN4*4-28)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.924	4.076	0.154	0.160
E	3.924	4.076	0.154	0.160
D1	2.200	2.400	0.087	0.094
E1	2.200	2.400	0.087	0.094
k	0.200MIN.		0.008MIN.	
b	0.150	0.250	0.006	0.010
e	0.400TYP.		0.016TYP.	
L	0.324	0.476	0.013	0.019

Classification Reflow Profiles

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max(Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60 -120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217 °C 60 -150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)* * within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsma x)	6°C/second max.
Time 25 °C to peak temperature	8 minutes max



Classification Profile

⚠CAUTION

Storage Conditions

1) This product should be used within 12 months after delivered. Store in manufacturer's package keeping the seal of aluminum coated baggage or tightly re-closed box with the following conditions. [Temperature:8℃...30℃,Humidity:30%...70% R.H.]

2) Keep the seal of aluminum coated baggage immediately before usage.

3) After breaking the seal of aluminum coated baggage, this product should be used within 1 week on the following conditions.
[Temperature:≤30℃, Humidity: ≤60% R.H.]